Path Summary

	Property	Value
1	From Node	std_2s60ES:inst|z_pwm_0:the_z_pwm_0|pwm_avalon_interface:z_pwm_0|pwm_task_logic:task_logic|lpm_divide:Div0|lpm_divide_jkm:auto_generated|sign_div_unsign_bnh:divider|alt_u_div_aaf:divider|add_sub_3_result_int[4]~8_OTERM505
2	To Node	std_2s60ES:inst|z_pwm_0:the_z_pwm_0|pwm_avalon_interface:z_pwm_0|pwm_task_logic:task_logic|lpm_divide:Div0|lpm_divide_jkm:auto_generated|sign_div_unsign_bnh:divider|alt_u_div_aaf:divider|StageOut[318]~181_OTERM535_Duplicate_Duplicate
3	Launch Clock	inst|the_cpu_pll|sd1|pll7|clk[2]
4	Latch Clock	inst|the_cpu_pll|sd1|pll7|clk[2]
5	Data Arrival Time	47.669
6	Data Required Time	20.668
7	Slack	-27.001 (VIOLATED)

Statistics

	Property	Value	Count	Total Delay	% of Total	Min	Max
1	Setup Relationship	20.000					
2	Clock Skew	0.326					
3	Data Delay	47.325					
4	Number of Logic Levels		165				
5	Physical Delays						
1	Arrival Path						
1	Clock						
1	IC		4	5.370	80	0.000	2.141
2	Cell		4	1.292	19	0.000	0.694
3	PLL Compensation		1	-6.318	0	-6.318	-6.318
2	Data						
1	IC		166	20.927	44	0.000	1.301
2	Cell		167	26.166	55	0.000	0.536
3	uTco		1	0.232	0	0.232	0.232
2	Required Path						
1	Clock						
1	IC		4	5.551	81	0.000	2.055
2	Cell		4	1.249	18	0.000	0.694
3	PLL Compensation		1	-6.512	0	-6.512	-6.512

Data Path

Data Arrival

	Total	Incr	RF	Type	Fanout	Location	Element
1	0.000	0.000					launch edge time
2	0.344	0.344					clock path
1	0.000	0.000					source latency
2	0.000	0.000			1	PIN_T2	sys_clk_in
3	0.000	0.000	RR	IC	1	IOIBUF_X0_Y14_N15	sys_clk_in~input|i
4	0.694	0.694	RR	CELL	2	IOIBUF_X0_Y14_N15	sys_clk_in~input|o
5	2.835	2.141	RR	IC	1	PLL_1	inst|the_cpu_pll|sd1|pll7|inclk[0]
6	-3.483	-6.318	RR	COMP	3	PLL_1	inst|the_cpu_pll|sd1|pll7|observablevcoout
7	-3.483	0.000	RR	CELL	1	PLL_1	inst|the_cpu_pll|sd1|pll7|clk[2]
8	-1.356	2.127	RR	IC	1	CLKCTRL_G3	inst|the_cpu_pll|sd1|wire_pll7_clk[2]~clkctrl|inclk[0]
9	-1.356	0.000	RR	CELL	7042	CLKCTRL_G3	inst|the_cpu_pll|sd1|wire_pll7_clk[2]~clkctrl|outclk
10	-0.254	1.102	RR	IC	1	FF_X32_Y12_N19	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_3_result_int[4]~8_NEW_REG504|clk
11	0.344	0.598	RR	CELL	1	FF_X32_Y12_N19	std_2s60ES:inst|z_pwm_0:the_z_pwm_0|pwm_avalon_interface:z_pwm_0|pwm_task_logic:task_logic|lpm_divide:Div0|lpm_divide_jkm:auto_generated|sign_div_unsign_bnh:divider|alt_u_div_aaf:divider|add_sub_3_result_int[4]~8_OTERM505
3	47.669	47.325					data path
1	0.576	0.232		uTco	1	FF_X32_Y12_N19	std_2s60ES:inst|z_pwm_0:the_z_pwm_0|pwm_avalon_interface:z_pwm_0|pwm_task_logic:task_logic|lpm_divide:Div0|lpm_divide_jkm:auto_generated|sign_div_unsign_bnh:divider|alt_u_div_aaf:divider|add_sub_3_result_int[4]~8_OTERM505
2	0.576	0.000	FF	CELL	3	FF_X32_Y12_N19	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_3_result_int[4]~8_NEW_REG504|q
3	0.977	0.401	FF	IC	1	LCCOMB_X32_Y12_N30	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|StageOut[51]~17|datab
4	1.333	0.356	FF	CELL	2	LCCOMB_X32_Y12_N30	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|StageOut[51]~17|combout
5	1.810	0.477	FF	IC	2	LCCOMB_X31_Y12_N6	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_4_result_int[1]~2|dataa
6	2.308	0.498	FR	CELL	1	LCCOMB_X31_Y12_N6	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_4_result_int[1]~2|cout
7	2.308	0.000	RR	IC	2	LCCOMB_X31_Y12_N8	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_4_result_int[2]~4|cin
8	2.374	0.066	RF	CELL	1	LCCOMB_X31_Y12_N8	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_4_result_int[2]~4|cout
9	2.374	0.000	FF	IC	2	LCCOMB_X31_Y12_N10	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_4_result_int[3]~6|cin
10	2.440	0.066	FR	CELL	1	LCCOMB_X31_Y12_N10	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_4_result_int[3]~6|cout
11	2.440	0.000	RR	IC	2	LCCOMB_X31_Y12_N12	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_4_result_int[4]~8|cin
12	2.506	0.066	RF	CELL	1	LCCOMB_X31_Y12_N12	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_4_result_int[4]~8|cout
13	2.506	0.000	FF	IC	1	LCCOMB_X31_Y12_N14	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_4_result_int[5]~10|cin
14	2.910	0.404	FR	CELL	6	LCCOMB_X31_Y12_N14	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_4_result_int[5]~10|combout
15	4.211	1.301	RR	IC	1	LCCOMB_X30_Y5_N8	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|StageOut[68]~22|datad
16	4.350	0.139	RF	CELL	2	LCCOMB_X30_Y5_N8	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|StageOut[68]~22|combout
17	4.629	0.279	FF	IC	2	LCCOMB_X30_Y5_N18	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_5_result_int[1]~2|datab
18	5.138	0.509	FR	CELL	1	LCCOMB_X30_Y5_N18	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_5_result_int[1]~2|cout
19	5.138	0.000	RR	IC	2	LCCOMB_X30_Y5_N20	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_5_result_int[2]~4|cin
20	5.204	0.066	RF	CELL	1	LCCOMB_X30_Y5_N20	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_5_result_int[2]~4|cout
21	5.204	0.000	FF	IC	2	LCCOMB_X30_Y5_N22	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_5_result_int[3]~6|cin
22	5.270	0.066	FR	CELL	1	LCCOMB_X30_Y5_N22	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_5_result_int[3]~6|cout
23	5.270	0.000	RR	IC	2	LCCOMB_X30_Y5_N24	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_5_result_int[4]~8|cin
24	5.336	0.066	RF	CELL	1	LCCOMB_X30_Y5_N24	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_5_result_int[4]~8|cout
25	5.336	0.000	FF	IC	2	LCCOMB_X30_Y5_N26	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_5_result_int[5]~10|cin
26	5.402	0.066	FR	CELL	1	LCCOMB_X30_Y5_N26	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_5_result_int[5]~10|cout
27	5.402	0.000	RR	IC	1	LCCOMB_X30_Y5_N28	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_5_result_int[6]~12|cin
28	5.938	0.536	RR	CELL	7	LCCOMB_X30_Y5_N28	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_5_result_int[6]~12|combout
29	6.225	0.287	RR	IC	1	LCCOMB_X30_Y5_N0	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|StageOut[86]~27|datad
30	6.380	0.155	RR	CELL	2	LCCOMB_X30_Y5_N0	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|StageOut[86]~27|combout
31	6.864	0.484	RR	IC	2	LCCOMB_X29_Y5_N6	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_6_result_int[2]~4|datab
32	7.336	0.472	RR	CELL	1	LCCOMB_X29_Y5_N6	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_6_result_int[2]~4|cout
33	7.336	0.000	RR	IC	2	LCCOMB_X29_Y5_N8	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_6_result_int[3]~6|cin
34	7.402	0.066	RF	CELL	1	LCCOMB_X29_Y5_N8	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_6_result_int[3]~6|cout
35	7.402	0.000	FF	IC	2	LCCOMB_X29_Y5_N10	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_6_result_int[4]~8|cin
36	7.468	0.066	FR	CELL	1	LCCOMB_X29_Y5_N10	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_6_result_int[4]~8|cout
37	7.468	0.000	RR	IC	2	LCCOMB_X29_Y5_N12	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_6_result_int[5]~10|cin
38	7.534	0.066	RF	CELL	1	LCCOMB_X29_Y5_N12	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_6_result_int[5]~10|cout
39	7.534	0.000	FF	IC	2	LCCOMB_X29_Y5_N14	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_6_result_int[6]~12|cin
40	7.600	0.066	FR	CELL	1	LCCOMB_X29_Y5_N14	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_6_result_int[6]~12|cout
41	7.600	0.000	RR	IC	1	LCCOMB_X29_Y5_N16	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_6_result_int[7]~14|cin
42	8.112	0.512	RF	CELL	8	LCCOMB_X29_Y5_N16	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_6_result_int[7]~14|combout
43	8.428	0.316	FF	IC	1	LCCOMB_X29_Y5_N30	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|StageOut[102]~35|datad
44	8.553	0.125	FF	CELL	2	LCCOMB_X29_Y5_N30	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|StageOut[102]~35|combout
45	9.304	0.751	FF	IC	2	LCCOMB_X29_Y8_N8	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_7_result_int[1]~2|dataa
46	9.802	0.498	FR	CELL	1	LCCOMB_X29_Y8_N8	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_7_result_int[1]~2|cout
47	9.802	0.000	RR	IC	2	LCCOMB_X29_Y8_N10	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_7_result_int[2]~4|cin
48	9.868	0.066	RF	CELL	1	LCCOMB_X29_Y8_N10	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_7_result_int[2]~4|cout
49	9.868	0.000	FF	IC	2	LCCOMB_X29_Y8_N12	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_7_result_int[3]~6|cin
50	9.934	0.066	FR	CELL	1	LCCOMB_X29_Y8_N12	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_7_result_int[3]~6|cout
51	9.934	0.000	RR	IC	2	LCCOMB_X29_Y8_N14	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_7_result_int[4]~8|cin
52	10.000	0.066	RF	CELL	1	LCCOMB_X29_Y8_N14	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_7_result_int[4]~8|cout
53	10.000	0.000	FF	IC	2	LCCOMB_X29_Y8_N16	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_7_result_int[5]~10|cin
54	10.066	0.066	FR	CELL	1	LCCOMB_X29_Y8_N16	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_7_result_int[5]~10|cout
55	10.066	0.000	RR	IC	2	LCCOMB_X29_Y8_N18	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_7_result_int[6]~12|cin
56	10.132	0.066	RF	CELL	1	LCCOMB_X29_Y8_N18	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_7_result_int[6]~12|cout
57	10.132	0.000	FF	IC	2	LCCOMB_X29_Y8_N20	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_7_result_int[7]~14|cin
58	10.198	0.066	FR	CELL	1	LCCOMB_X29_Y8_N20	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_7_result_int[7]~14|cout
59	10.198	0.000	RR	IC	1	LCCOMB_X29_Y8_N22	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_7_result_int[8]~16|cin
60	10.734	0.536	RR	CELL	11	LCCOMB_X29_Y8_N22	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_7_result_int[8]~16|combout
61	11.003	0.269	RR	IC	1	LCCOMB_X29_Y8_N30	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|StageOut[120]~42|datac
62	11.290	0.287	RR	CELL	2	LCCOMB_X29_Y8_N30	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|StageOut[120]~42|combout
63	12.036	0.746	RR	IC	2	LCCOMB_X29_Y11_N10	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_8_result_int[2]~4|dataa
64	12.502	0.466	RR	CELL	1	LCCOMB_X29_Y11_N10	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_8_result_int[2]~4|cout
65	12.502	0.000	RR	IC	2	LCCOMB_X29_Y11_N12	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_8_result_int[3]~6|cin
66	12.568	0.066	RF	CELL	1	LCCOMB_X29_Y11_N12	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_8_result_int[3]~6|cout
67	12.568	0.000	FF	IC	2	LCCOMB_X29_Y11_N14	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_8_result_int[4]~8|cin
68	12.634	0.066	FR	CELL	1	LCCOMB_X29_Y11_N14	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_8_result_int[4]~8|cout
69	12.634	0.000	RR	IC	2	LCCOMB_X29_Y11_N16	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_8_result_int[5]~10|cin
70	12.700	0.066	RF	CELL	1	LCCOMB_X29_Y11_N16	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_8_result_int[5]~10|cout
71	12.700	0.000	FF	IC	2	LCCOMB_X29_Y11_N18	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_8_result_int[6]~12|cin
72	12.766	0.066	FR	CELL	1	LCCOMB_X29_Y11_N18	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_8_result_int[6]~12|cout
73	12.766	0.000	RR	IC	2	LCCOMB_X29_Y11_N20	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_8_result_int[7]~14|cin
74	12.832	0.066	RF	CELL	1	LCCOMB_X29_Y11_N20	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_8_result_int[7]~14|cout
75	12.832	0.000	FF	IC	2	LCCOMB_X29_Y11_N22	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_8_result_int[8]~16|cin
76	12.898	0.066	FR	CELL	1	LCCOMB_X29_Y11_N22	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_8_result_int[8]~16|cout
77	12.898	0.000	RR	IC	1	LCCOMB_X29_Y11_N24	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_8_result_int[9]~18|cin
78	13.410	0.512	RF	CELL	14	LCCOMB_X29_Y11_N24	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_8_result_int[9]~18|combout
79	14.407	0.997	FF	IC	1	LCCOMB_X30_Y8_N24	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|StageOut[141]~47_Duplicate|datad
80	14.557	0.150	FR	CELL	1	LCCOMB_X30_Y8_N24	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|StageOut[141]~47_Duplicate|combout
81	15.275	0.718	RR	IC	2	LCCOMB_X30_Y11_N18	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_9_result_int[6]~12|datab
82	15.747	0.472	RR	CELL	1	LCCOMB_X30_Y11_N18	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_9_result_int[6]~12|cout
83	15.747	0.000	RR	IC	2	LCCOMB_X30_Y11_N20	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_9_result_int[7]~14|cin

	Total	Incr	RF	Type	Fanout	Location	Element
84	15.813	0.066	RF	CELL	1	LCCOMB_X30_Y11_N20	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_9_result_int[7]~14|cout
85	15.813	0.000	FF	IC	2	LCCOMB_X30_Y11_N22	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_9_result_int[8]~16|cin
86	15.879	0.066	FR	CELL	1	LCCOMB_X30_Y11_N22	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_9_result_int[8]~16|cout
87	15.879	0.000	RR	IC	2	LCCOMB_X30_Y11_N24	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_9_result_int[9]~18|cin
88	15.945	0.066	RF	CELL	1	LCCOMB_X30_Y11_N24	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_9_result_int[9]~18|cout
89	15.945	0.000	FF	IC	1	LCCOMB_X30_Y11_N26	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_9_result_int[10]~20|cin
90	16.379	0.434	FF	CELL	18	LCCOMB_X30_Y11_N26	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_9_result_int[10]~20|combout
91	16.672	0.293	FF	IC	1	LCCOMB_X30_Y11_N4	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|StageOut[154]~61|datac
92	16.933	0.261	FR	CELL	2	LCCOMB_X30_Y11_N4	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|StageOut[154]~61|combout
93	17.645	0.712	RR	IC	2	LCCOMB_X32_Y11_N8	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_10_result_int[2]~4|datab
94	18.117	0.472	RR	CELL	1	LCCOMB_X32_Y11_N8	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_10_result_int[2]~4|cout
95	18.117	0.000	RR	IC	2	LCCOMB_X32_Y11_N10	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_10_result_int[3]~6|cin
96	18.183	0.066	RF	CELL	1	LCCOMB_X32_Y11_N10	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_10_result_int[3]~6|cout
97	18.183	0.000	FF	IC	2	LCCOMB_X32_Y11_N12	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_10_result_int[4]~8|cin
98	18.249	0.066	FR	CELL	1	LCCOMB_X32_Y11_N12	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_10_result_int[4]~8|cout
99	18.249	0.000	RR	IC	2	LCCOMB_X32_Y11_N14	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_10_result_int[5]~10|cin
100	18.315	0.066	RF	CELL	1	LCCOMB_X32_Y11_N14	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_10_result_int[5]~10|cout
101	18.315	0.000	FF	IC	2	LCCOMB_X32_Y11_N16	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_10_result_int[6]~12|cin
102	18.381	0.066	FR	CELL	1	LCCOMB_X32_Y11_N16	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_10_result_int[6]~12|cout
103	18.381	0.000	RR	IC	2	LCCOMB_X32_Y11_N18	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_10_result_int[7]~14|cin
104	18.447	0.066	RF	CELL	1	LCCOMB_X32_Y11_N18	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_10_result_int[7]~14|cout
105	18.447	0.000	FF	IC	2	LCCOMB_X32_Y11_N20	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_10_result_int[8]~16|cin
106	18.513	0.066	FR	CELL	1	LCCOMB_X32_Y11_N20	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_10_result_int[8]~16|cout
107	18.513	0.000	RR	IC	2	LCCOMB_X32_Y11_N22	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_10_result_int[9]~18|cin
108	18.579	0.066	RF	CELL	1	LCCOMB_X32_Y11_N22	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_10_result_int[9]~18|cout
109	18.579	0.000	FF	IC	2	LCCOMB_X32_Y11_N24	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_10_result_int[10]~20|cin
110	18.645	0.066	FR	CELL	1	LCCOMB_X32_Y11_N24	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_10_result_int[10]~20|cout
111	18.645	0.000	RR	IC	1	LCCOMB_X32_Y11_N26	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_10_result_int[11]~22|cin
112	19.157	0.512	RF	CELL	22	LCCOMB_X32_Y11_N26	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_10_result_int[11]~22|combout
113	19.712	0.555	FF	IC	1	LCCOMB_X31_Y11_N30	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|StageOut[172]~71|datad
114	19.837	0.125	FF	CELL	4	LCCOMB_X31_Y11_N30	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|StageOut[172]~71|combout
115	20.505	0.668	FF	IC	2	LCCOMB_X32_Y10_N8	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_11_result_int[3]~6|datab
116	21.014	0.509	FR	CELL	1	LCCOMB_X32_Y10_N8	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_11_result_int[3]~6|cout
117	21.014	0.000	RR	IC	2	LCCOMB_X32_Y10_N10	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_11_result_int[4]~8|cin
118	21.080	0.066	RF	CELL	1	LCCOMB_X32_Y10_N10	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_11_result_int[4]~8|cout
119	21.080	0.000	FF	IC	2	LCCOMB_X32_Y10_N12	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_11_result_int[5]~10|cin
120	21.146	0.066	FR	CELL	1	LCCOMB_X32_Y10_N12	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_11_result_int[5]~10|cout
121	21.146	0.000	RR	IC	2	LCCOMB_X32_Y10_N14	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_11_result_int[6]~12|cin
122	21.212	0.066	RF	CELL	1	LCCOMB_X32_Y10_N14	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_11_result_int[6]~12|cout
123	21.212	0.000	FF	IC	2	LCCOMB_X32_Y10_N16	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_11_result_int[7]~14|cin
124	21.278	0.066	FR	CELL	1	LCCOMB_X32_Y10_N16	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_11_result_int[7]~14|cout
125	21.278	0.000	RR	IC	2	LCCOMB_X32_Y10_N18	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_11_result_int[8]~16|cin
126	21.344	0.066	RF	CELL	1	LCCOMB_X32_Y10_N18	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_11_result_int[8]~16|cout
127	21.344	0.000	FF	IC	2	LCCOMB_X32_Y10_N20	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_11_result_int[9]~18|cin
128	21.410	0.066	FR	CELL	1	LCCOMB_X32_Y10_N20	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_11_result_int[9]~18|cout
129	21.410	0.000	RR	IC	2	LCCOMB_X32_Y10_N22	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_11_result_int[10]~20|cin
130	21.476	0.066	RF	CELL	1	LCCOMB_X32_Y10_N22	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_11_result_int[10]~20|cout
131	21.476	0.000	FF	IC	2	LCCOMB_X32_Y10_N24	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_11_result_int[11]~22|cin
132	21.542	0.066	FR	CELL	1	LCCOMB_X32_Y10_N24	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_11_result_int[11]~22|cout
133	21.542	0.000	RR	IC	1	LCCOMB_X32_Y10_N26	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_11_result_int[12]~24|cin
134	22.078	0.536	RR	CELL	35	LCCOMB_X32_Y10_N26	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_11_result_int[12]~24|combout
135	22.590	0.512	RR	IC	1	LCCOMB_X31_Y10_N22	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|StageOut[187]~85_Duplicate|datad
136	22.745	0.155	RR	CELL	2	LCCOMB_X31_Y10_N22	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|StageOut[187]~85_Duplicate|combout
137	23.214	0.469	RR	IC	2	LCCOMB_X30_Y10_N4	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_12_result_int[1]~2|datab
138	23.586	0.372	RF	CELL	1	LCCOMB_X30_Y10_N4	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_12_result_int[1]~2|cout
139	23.586	0.000	FF	IC	2	LCCOMB_X30_Y10_N6	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_12_result_int[2]~4|cin
140	23.652	0.066	FR	CELL	1	LCCOMB_X30_Y10_N6	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_12_result_int[2]~4|cout
141	23.652	0.000	RR	IC	2	LCCOMB_X30_Y10_N8	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_12_result_int[3]~6|cin
142	23.718	0.066	RF	CELL	1	LCCOMB_X30_Y10_N8	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_12_result_int[3]~6|cout
143	23.718	0.000	FF	IC	2	LCCOMB_X30_Y10_N10	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_12_result_int[4]~8|cin
144	23.784	0.066	FR	CELL	1	LCCOMB_X30_Y10_N10	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_12_result_int[4]~8|cout
145	23.784	0.000	RR	IC	2	LCCOMB_X30_Y10_N12	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_12_result_int[5]~10|cin
146	23.850	0.066	RF	CELL	1	LCCOMB_X30_Y10_N12	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_12_result_int[5]~10|cout
147	23.850	0.000	FF	IC	2	LCCOMB_X30_Y10_N14	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_12_result_int[6]~12|cin
148	23.916	0.066	FR	CELL	1	LCCOMB_X30_Y10_N14	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_12_result_int[6]~12|cout
149	23.916	0.000	RR	IC	2	LCCOMB_X30_Y10_N16	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_12_result_int[7]~14|cin
150	23.982	0.066	RF	CELL	1	LCCOMB_X30_Y10_N16	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_12_result_int[7]~14|cout
151	23.982	0.000	FF	IC	2	LCCOMB_X30_Y10_N18	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_12_result_int[8]~16|cin
152	24.048	0.066	FR	CELL	1	LCCOMB_X30_Y10_N18	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_12_result_int[8]~16|cout
153	24.048	0.000	RR	IC	2	LCCOMB_X30_Y10_N20	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_12_result_int[9]~18|cin
154	24.114	0.066	RF	CELL	1	LCCOMB_X30_Y10_N20	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_12_result_int[9]~18|cout
155	24.114	0.000	FF	IC	2	LCCOMB_X30_Y10_N22	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_12_result_int[10]~20|cin
156	24.180	0.066	FR	CELL	1	LCCOMB_X30_Y10_N22	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_12_result_int[10]~20|cout
157	24.180	0.000	RR	IC	2	LCCOMB_X30_Y10_N24	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_12_result_int[11]~22|cin
158	24.246	0.066	RF	CELL	1	LCCOMB_X30_Y10_N24	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_12_result_int[11]~22|cout
159	24.246	0.000	FF	IC	2	LCCOMB_X30_Y10_N26	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_12_result_int[12]~24|cin
160	24.312	0.066	FR	CELL	1	LCCOMB_X30_Y10_N26	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_12_result_int[12]~24|cout
161	24.312	0.000	RR	IC	1	LCCOMB_X30_Y10_N28	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_12_result_int[13]~26|cin
162	24.824	0.512	RF	CELL	34	LCCOMB_X30_Y10_N28	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_12_result_int[13]~26|combout
163	25.664	0.840	FF	IC	1	LCCOMB_X31_Y9_N26	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|StageOut[204]~98_Duplicate_621|datac
164	25.944	0.280	FF	CELL	1	LCCOMB_X31_Y9_N26	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|StageOut[204]~98_Duplicate_621|combout
165	26.396	0.452	FF	IC	2	LCCOMB_X30_Y9_N2	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_13_result_int[1]~2|datab
166	26.905	0.509	FR	CELL	1	LCCOMB_X30_Y9_N2	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_13_result_int[1]~2|cout
167	26.905	0.000	RR	IC	2	LCCOMB_X30_Y9_N4	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_13_result_int[2]~4|cin
168	26.971	0.066	RF	CELL	1	LCCOMB_X30_Y9_N4	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_13_result_int[2]~4|cout
169	26.971	0.000	FF	IC	2	LCCOMB_X30_Y9_N6	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_13_result_int[3]~6|cin
170	27.037	0.066	FR	CELL	1	LCCOMB_X30_Y9_N6	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_13_result_int[3]~6|cout
171	27.037	0.000	RR	IC	2	LCCOMB_X30_Y9_N8	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_13_result_int[4]~8|cin
172	27.103	0.066	RF	CELL	1	LCCOMB_X30_Y9_N8	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_13_result_int[4]~8|cout
173	27.103	0.000	FF	IC	2	LCCOMB_X30_Y9_N10	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_13_result_int[5]~10|cin
174	27.169	0.066	FR	CELL	1	LCCOMB_X30_Y9_N10	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_13_result_int[5]~10|cout
175	27.169	0.000	RR	IC	2	LCCOMB_X30_Y9_N12	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_13_result_int[6]~12|cin
176	27.235	0.066	RF	CELL	1	LCCOMB_X30_Y9_N12	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_13_result_int[6]~12|cout
177	27.235	0.000	FF	IC	2	LCCOMB_X30_Y9_N14	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_13_result_int[7]~14|cin
178	27.301	0.066	FR	CELL	1	LCCOMB_X30_Y9_N14	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_13_result_int[7]~14|cout
179	27.301	0.000	RR	IC	2	LCCOMB_X30_Y9_N16	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_13_result_int[8]~16|cin
180	27.367	0.066	RF	CELL	1	LCCOMB_X30_Y9_N16	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_13_result_int[8]~16|cout
181	27.367	0.000	FF	IC	2	LCCOMB_X30_Y9_N18	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_13_result_int[9]~18|cin
182	27.433	0.066	FR	CELL	1	LCCOMB_X30_Y9_N18	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_13_result_int[9]~18|cout
183	27.433	0.000	RR	IC	2	LCCOMB_X30_Y9_N20	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_13_result_int[10]~20|cin
184	27.499	0.066	RF	CELL	1	LCCOMB_X30_Y9_N20	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_13_result_int[10]~20|cout
185	27.499	0.000	FF	IC	2	LCCOMB_X30_Y9_N22	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_13_result_int[11]~22|cin
186	27.565	0.066	FR	CELL	1	LCCOMB_X30_Y9_N22	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_13_result_int[11]~22|cout
187	27.565	0.000	RR	IC	2	LCCOMB_X30_Y9_N24	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_13_result_int[12]~24|cin
188	27.631	0.066	RF	CELL	1	LCCOMB_X30_Y9_N24	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_13_result_int[12]~24|cout
189	27.631	0.000	FF	IC	2	LCCOMB_X30_Y9_N26	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_13_result_int[13]~26|cin
190	27.697	0.066	FR	CELL	1	LCCOMB_X30_Y9_N26	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_13_result_int[13]~26|cout
191	27.697	0.000	RR	IC	1	LCCOMB_X30_Y9_N28	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_13_result_int[14]~28|cin
192	28.233	0.536	RR	CELL	33	LCCOMB_X30_Y9_N28	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_13_result_int[14]~28|combout
193	29.186	0.953	RR	IC	1	LCCOMB_X29_Y10_N26	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|StageOut[225]~108_Duplicate|datac
194	29.473	0.287	RR	CELL	1	LCCOMB_X29_Y10_N26	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|StageOut[225]~108_Duplicate|combout
195	30.436	0.963	RR	IC	2	LCCOMB_X32_Y8_N10	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_14_result_int[5]~10|datab
196	30.808	0.372	RF	CELL	1	LCCOMB_X32_Y8_N10	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_14_result_int[5]~10|cout
197	30.808	0.000	FF	IC	2	LCCOMB_X32_Y8_N12	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_14_result_int[6]~12|cin
198	30.874	0.066	FR	CELL	1	LCCOMB_X32_Y8_N12	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_14_result_int[6]~12|cout
199	30.874	0.000	RR	IC	2	LCCOMB_X32_Y8_N14	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_14_result_int[7]~14|cin
200	30.940	0.066	RF	CELL	1	LCCOMB_X32_Y8_N14	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_14_result_int[7]~14|cout
201	30.940	0.000	FF	IC	2	LCCOMB_X32_Y8_N16	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_14_result_int[8]~16|cin
202	31.006	0.066	FR	CELL	1	LCCOMB_X32_Y8_N16	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_14_result_int[8]~16|cout
203	31.006	0.000	RR	IC	2	LCCOMB_X32_Y8_N18	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_14_result_int[9]~18|cin
204	31.072	0.066	RF	CELL	1	LCCOMB_X32_Y8_N18	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_14_result_int[9]~18|cout
205	31.072	0.000	FF	IC	2	LCCOMB_X32_Y8_N20	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_14_result_int[10]~20|cin
206	31.138	0.066	FR	CELL	1	LCCOMB_X32_Y8_N20	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_14_result_int[10]~20|cout
207	31.138	0.000	RR	IC	2	LCCOMB_X32_Y8_N22	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_14_result_int[11]~22|cin
208	31.204	0.066	RF	CELL	1	LCCOMB_X32_Y8_N22	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_14_result_int[11]~22|cout
209	31.204	0.000	FF	IC	2	LCCOMB_X32_Y8_N24	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_14_result_int[12]~24|cin
210	31.270	0.066	FR	CELL	1	LCCOMB_X32_Y8_N24	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_14_result_int[12]~24|cout
211	31.270	0.000	RR	IC	2	LCCOMB_X32_Y8_N26	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_14_result_int[13]~26|cin
212	31.336	0.066	RF	CELL	1	LCCOMB_X32_Y8_N26	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_14_result_int[13]~26|cout
213	31.336	0.000	FF	IC	2	LCCOMB_X32_Y8_N28	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_14_result_int[14]~28|cin
214	31.402	0.066	FR	CELL	1	LCCOMB_X32_Y8_N28	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_14_result_int[14]~28|cout
215	31.402	0.000	RR	IC	1	LCCOMB_X32_Y8_N30	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_14_result_int[15]~30|cin
216	31.914	0.512	RF	CELL	33	LCCOMB_X32_Y8_N30	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_14_result_int[15]~30|combout
217	32.763	0.849	FF	IC	1	LCCOMB_X33_Y10_N4	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|StageOut[244]~121_Duplicate|datad
218	32.888	0.125	FF	CELL	3	LCCOMB_X33_Y10_N4	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|StageOut[244]~121_Duplicate|combout

	Total	Incr	RF	Type	Fanout	Location	Element
219	33.651	0.763	FF	IC	2	LCCOMB_X33_Y9_N30	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_15_result_int[7]~14|dataa
220	34.149	0.498	FR	CELL	1	LCCOMB_X33_Y9_N30	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_15_result_int[7]~14|cout
221	34.149	0.000	RR	IC	2	LCCOMB_X33_Y8_N0	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_15_result_int[8]~16|cin
222	34.215	0.066	RF	CELL	1	LCCOMB_X33_Y8_N0	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_15_result_int[8]~16|cout
223	34.215	0.000	FF	IC	2	LCCOMB_X33_Y8_N2	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_15_result_int[9]~18|cin
224	34.281	0.066	FR	CELL	1	LCCOMB_X33_Y8_N2	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_15_result_int[9]~18|cout
225	34.281	0.000	RR	IC	2	LCCOMB_X33_Y8_N4	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_15_result_int[10]~20|cin
226	34.347	0.066	RF	CELL	1	LCCOMB_X33_Y8_N4	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_15_result_int[10]~20|cout
227	34.347	0.000	FF	IC	2	LCCOMB_X33_Y8_N6	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_15_result_int[11]~22|cin
228	34.413	0.066	FR	CELL	1	LCCOMB_X33_Y8_N6	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_15_result_int[11]~22|cout
229	34.413	0.000	RR	IC	2	LCCOMB_X33_Y8_N8	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_15_result_int[12]~24|cin
230	34.479	0.066	RF	CELL	1	LCCOMB_X33_Y8_N8	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_15_result_int[12]~24|cout
231	34.479	0.000	FF	IC	2	LCCOMB_X33_Y8_N10	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_15_result_int[13]~26|cin
232	34.545	0.066	FR	CELL	1	LCCOMB_X33_Y8_N10	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_15_result_int[13]~26|cout
233	34.545	0.000	RR	IC	2	LCCOMB_X33_Y8_N12	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_15_result_int[14]~28|cin
234	34.611	0.066	RF	CELL	1	LCCOMB_X33_Y8_N12	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_15_result_int[14]~28|cout
235	34.611	0.000	FF	IC	2	LCCOMB_X33_Y8_N14	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_15_result_int[15]~30|cin
236	34.677	0.066	FR	CELL	1	LCCOMB_X33_Y8_N14	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_15_result_int[15]~30|cout
237	34.677	0.000	RR	IC	1	LCCOMB_X33_Y8_N16	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_15_result_int[16]~32|cin
238	35.213	0.536	RR	CELL	36	LCCOMB_X33_Y8_N16	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_15_result_int[16]~32|combout
239	35.980	0.767	RR	IC	1	LCCOMB_X33_Y9_N2	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|StageOut[256]~143_Duplicate|datad
240	36.135	0.155	RR	CELL	1	LCCOMB_X33_Y9_N2	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|StageOut[256]~143_Duplicate|combout
241	36.768	0.633	RR	IC	2	LCCOMB_X37_Y9_N18	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_16_result_int[2]~4|datab
242	37.240	0.472	RR	CELL	1	LCCOMB_X37_Y9_N18	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_16_result_int[2]~4|cout
243	37.240	0.000	RR	IC	2	LCCOMB_X37_Y9_N20	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_16_result_int[3]~6|cin
244	37.306	0.066	RF	CELL	1	LCCOMB_X37_Y9_N20	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_16_result_int[3]~6|cout
245	37.306	0.000	FF	IC	2	LCCOMB_X37_Y9_N22	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_16_result_int[4]~8|cin
246	37.372	0.066	FR	CELL	1	LCCOMB_X37_Y9_N22	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_16_result_int[4]~8|cout
247	37.372	0.000	RR	IC	2	LCCOMB_X37_Y9_N24	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_16_result_int[5]~10|cin
248	37.438	0.066	RF	CELL	1	LCCOMB_X37_Y9_N24	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_16_result_int[5]~10|cout
249	37.438	0.000	FF	IC	2	LCCOMB_X37_Y9_N26	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_16_result_int[6]~12|cin
250	37.504	0.066	FR	CELL	1	LCCOMB_X37_Y9_N26	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_16_result_int[6]~12|cout
251	37.504	0.000	RR	IC	2	LCCOMB_X37_Y9_N28	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_16_result_int[7]~14|cin
252	37.570	0.066	RF	CELL	1	LCCOMB_X37_Y9_N28	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_16_result_int[7]~14|cout
253	37.570	0.000	FF	IC	2	LCCOMB_X37_Y9_N30	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_16_result_int[8]~16|cin
254	37.636	0.066	FR	CELL	1	LCCOMB_X37_Y9_N30	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_16_result_int[8]~16|cout
255	37.636	0.000	RR	IC	2	LCCOMB_X37_Y8_N0	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_16_result_int[9]~18|cin
256	37.702	0.066	RF	CELL	1	LCCOMB_X37_Y8_N0	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_16_result_int[9]~18|cout
257	37.702	0.000	FF	IC	2	LCCOMB_X37_Y8_N2	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_16_result_int[10]~20|cin
258	37.768	0.066	FR	CELL	1	LCCOMB_X37_Y8_N2	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_16_result_int[10]~20|cout
259	37.768	0.000	RR	IC	2	LCCOMB_X37_Y8_N4	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_16_result_int[11]~22|cin
260	37.834	0.066	RF	CELL	1	LCCOMB_X37_Y8_N4	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_16_result_int[11]~22|cout
261	37.834	0.000	FF	IC	2	LCCOMB_X37_Y8_N6	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_16_result_int[12]~24|cin
262	37.900	0.066	FR	CELL	1	LCCOMB_X37_Y8_N6	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_16_result_int[12]~24|cout
263	37.900	0.000	RR	IC	2	LCCOMB_X37_Y8_N8	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_16_result_int[13]~26|cin
264	37.966	0.066	RF	CELL	1	LCCOMB_X37_Y8_N8	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_16_result_int[13]~26|cout
265	37.966	0.000	FF	IC	2	LCCOMB_X37_Y8_N10	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_16_result_int[14]~28|cin
266	38.032	0.066	FR	CELL	1	LCCOMB_X37_Y8_N10	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_16_result_int[14]~28|cout
267	38.032	0.000	RR	IC	2	LCCOMB_X37_Y8_N12	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_16_result_int[15]~30|cin
268	38.098	0.066	RF	CELL	1	LCCOMB_X37_Y8_N12	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_16_result_int[15]~30|cout
269	38.098	0.000	FF	IC	1	LCCOMB_X37_Y8_N14	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_16_result_int[16]~33|cin
270	38.164	0.066	FR	CELL	1	LCCOMB_X37_Y8_N14	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_16_result_int[16]~33|cout
271	38.164	0.000	RR	IC	1	LCCOMB_X37_Y8_N16	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_16_result_int[17]~34|cin
272	38.676	0.512	RF	CELL	34	LCCOMB_X37_Y8_N16	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_16_result_int[17]~34|combout
273	39.560	0.884	FF	IC	1	LCCOMB_X36_Y9_N12	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|StageOut[272]~160_Duplicate_Duplicate|datac
274	39.841	0.281	FF	CELL	2	LCCOMB_X36_Y9_N12	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|StageOut[272]~160_Duplicate_Duplicate|combout
275	40.139	0.298	FF	IC	2	LCCOMB_X36_Y9_N16	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_17_result_int[1]~2|dataa
276	40.637	0.498	FR	CELL	1	LCCOMB_X36_Y9_N16	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_17_result_int[1]~2|cout
277	40.637	0.000	RR	IC	2	LCCOMB_X36_Y9_N18	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_17_result_int[2]~4|cin
278	40.703	0.066	RF	CELL	1	LCCOMB_X36_Y9_N18	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_17_result_int[2]~4|cout
279	40.703	0.000	FF	IC	2	LCCOMB_X36_Y9_N20	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_17_result_int[3]~6|cin
280	40.769	0.066	FR	CELL	1	LCCOMB_X36_Y9_N20	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_17_result_int[3]~6|cout
281	40.769	0.000	RR	IC	2	LCCOMB_X36_Y9_N22	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_17_result_int[4]~8|cin
282	40.835	0.066	RF	CELL	1	LCCOMB_X36_Y9_N22	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_17_result_int[4]~8|cout
283	40.835	0.000	FF	IC	2	LCCOMB_X36_Y9_N24	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_17_result_int[5]~10|cin
284	40.901	0.066	FR	CELL	1	LCCOMB_X36_Y9_N24	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_17_result_int[5]~10|cout
285	40.901	0.000	RR	IC	2	LCCOMB_X36_Y9_N26	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_17_result_int[6]~12|cin
286	40.967	0.066	RF	CELL	1	LCCOMB_X36_Y9_N26	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_17_result_int[6]~12|cout
287	40.967	0.000	FF	IC	2	LCCOMB_X36_Y9_N28	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_17_result_int[7]~14|cin
288	41.033	0.066	FR	CELL	1	LCCOMB_X36_Y9_N28	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_17_result_int[7]~14|cout
289	41.033	0.000	RR	IC	2	LCCOMB_X36_Y9_N30	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_17_result_int[8]~16|cin
290	41.099	0.066	RF	CELL	1	LCCOMB_X36_Y9_N30	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_17_result_int[8]~16|cout
291	41.099	0.000	FF	IC	2	LCCOMB_X36_Y8_N0	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_17_result_int[9]~18|cin
292	41.165	0.066	FR	CELL	1	LCCOMB_X36_Y8_N0	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_17_result_int[9]~18|cout
293	41.165	0.000	RR	IC	2	LCCOMB_X36_Y8_N2	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_17_result_int[10]~20|cin
294	41.231	0.066	RF	CELL	1	LCCOMB_X36_Y8_N2	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_17_result_int[10]~20|cout
295	41.231	0.000	FF	IC	2	LCCOMB_X36_Y8_N4	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_17_result_int[11]~22|cin
296	41.297	0.066	FR	CELL	1	LCCOMB_X36_Y8_N4	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_17_result_int[11]~22|cout
297	41.297	0.000	RR	IC	2	LCCOMB_X36_Y8_N6	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_17_result_int[12]~24|cin
298	41.363	0.066	RF	CELL	1	LCCOMB_X36_Y8_N6	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_17_result_int[12]~24|cout
299	41.363	0.000	FF	IC	2	LCCOMB_X36_Y8_N8	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_17_result_int[13]~26|cin
300	41.429	0.066	FR	CELL	1	LCCOMB_X36_Y8_N8	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_17_result_int[13]~26|cout
301	41.429	0.000	RR	IC	2	LCCOMB_X36_Y8_N10	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_17_result_int[14]~28|cin
302	41.495	0.066	RF	CELL	1	LCCOMB_X36_Y8_N10	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_17_result_int[14]~28|cout
303	41.495	0.000	FF	IC	2	LCCOMB_X36_Y8_N12	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_17_result_int[15]~30|cin
304	41.561	0.066	FR	CELL	1	LCCOMB_X36_Y8_N12	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_17_result_int[15]~30|cout
305	41.561	0.000	RR	IC	1	LCCOMB_X36_Y8_N14	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_17_result_int[16]~33|cin
306	41.627	0.066	RF	CELL	1	LCCOMB_X36_Y8_N14	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_17_result_int[16]~33|cout
307	41.627	0.000	FF	IC	1	LCCOMB_X36_Y8_N16	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_17_result_int[17]~34|cin
308	42.031	0.404	FR	CELL	31	LCCOMB_X36_Y8_N16	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_17_result_int[17]~34|combout
309	43.110	1.079	RR	IC	1	LCCOMB_X36_Y5_N10	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|StageOut[296]~170_Duplicate|datad
310	43.265	0.155	RR	CELL	2	LCCOMB_X36_Y5_N10	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|StageOut[296]~170_Duplicate|combout
311	43.987	0.722	RR	IC	2	LCCOMB_X35_Y9_N30	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_18_result_int[8]~16|datab
312	44.459	0.472	RR	CELL	1	LCCOMB_X35_Y9_N30	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_18_result_int[8]~16|cout
313	44.459	0.000	RR	IC	2	LCCOMB_X35_Y8_N0	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_18_result_int[9]~18|cin
314	44.525	0.066	RF	CELL	1	LCCOMB_X35_Y8_N0	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_18_result_int[9]~18|cout
315	44.525	0.000	FF	IC	2	LCCOMB_X35_Y8_N2	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_18_result_int[10]~20|cin
316	44.591	0.066	FR	CELL	1	LCCOMB_X35_Y8_N2	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_18_result_int[10]~20|cout
317	44.591	0.000	RR	IC	2	LCCOMB_X35_Y8_N4	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_18_result_int[11]~22|cin
318	44.657	0.066	RF	CELL	1	LCCOMB_X35_Y8_N4	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_18_result_int[11]~22|cout
319	44.657	0.000	FF	IC	2	LCCOMB_X35_Y8_N6	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_18_result_int[12]~24|cin
320	44.723	0.066	FR	CELL	1	LCCOMB_X35_Y8_N6	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_18_result_int[12]~24|cout
321	44.723	0.000	RR	IC	2	LCCOMB_X35_Y8_N8	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_18_result_int[13]~26|cin
322	44.789	0.066	RF	CELL	1	LCCOMB_X35_Y8_N8	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_18_result_int[13]~26|cout
323	44.789	0.000	FF	IC	2	LCCOMB_X35_Y8_N10	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_18_result_int[14]~28|cin
324	44.855	0.066	FR	CELL	1	LCCOMB_X35_Y8_N10	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_18_result_int[14]~28|cout
325	44.855	0.000	RR	IC	2	LCCOMB_X35_Y8_N12	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_18_result_int[15]~30|cin
326	44.921	0.066	RF	CELL	1	LCCOMB_X35_Y8_N12	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_18_result_int[15]~30|cout
327	44.921	0.000	FF	IC	1	LCCOMB_X35_Y8_N14	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_18_result_int[16]~33|cin
328	44.987	0.066	FR	CELL	1	LCCOMB_X35_Y8_N14	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_18_result_int[16]~33|cout
329	44.987	0.000	RR	IC	1	LCCOMB_X35_Y8_N16	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_18_result_int[17]~34|cin
330	45.499	0.512	RF	CELL	19	LCCOMB_X35_Y8_N16	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|add_sub_18_result_int[17]~34|combout
331	46.260	0.761	FF	IC	1	LCCOMB_X36_Y7_N8	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|StageOut[318]~181|datac
332	46.540	0.280	FF	CELL	2	LCCOMB_X36_Y7_N8	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|StageOut[318]~181|combout
333	47.268	0.728	FF	IC	1	FF_X35_Y11_N9	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|StageOut[318]~181_NEW_REG534_Duplicate_Duplicate|asdata
334	47.669	0.401	FF	CELL	1	FF_X35_Y11_N9	std_2s60ES:inst|z_pwm_0:the_z_pwm_0|pwm_avalon_interface:z_pwm_0|pwm_task_logic:task_logic|lpm_divide:Div0|lpm_divide_jkm:auto_generated|sign_div_unsign_bnh:divider|alt_u_div_aaf:divider|StageOut[318]~181_OTERM535_Duplicate_Duplicate

Data Required

	Total	Incr	RF	Type	Fanout	Location	Element
1	20.000	20.000					latch edge time
2	20.670	0.670					clock path
1	20.000	0.000					source latency
2	20.000	0.000			1	PIN_T2	sys_clk_in
3	20.000	0.000	RR	IC	1	IOIBUF_X0_Y14_N15	sys_clk_in~input|i
4	20.694	0.694	RR	CELL	2	IOIBUF_X0_Y14_N15	sys_clk_in~input|o
5	22.749	2.055	RR	IC	1	PLL_1	inst|the_cpu_pll|sd1|pll7|inclk[0]
6	16.237	-6.512	RR	COMP	3	PLL_1	inst|the_cpu_pll|sd1|pll7|observablevcoout
7	16.237	0.000	RR	CELL	1	PLL_1	inst|the_cpu_pll|sd1|pll7|clk[2]
8	18.279	2.042	RR	IC	1	CLKCTRL_G3	inst|the_cpu_pll|sd1|wire_pll7_clk[2]~clkctrl|inclk[0]
9	18.279	0.000	RR	CELL	7042	CLKCTRL_G3	inst|the_cpu_pll|sd1|wire_pll7_clk[2]~clkctrl|outclk
10	19.733	1.454	RR	IC	1	FF_X35_Y11_N9	inst|the_z_pwm_0|z_pwm_0|task_logic|Div0|auto_generated|divider|divider|StageOut[318]~181_NEW_REG534_Duplicate_Duplicate|clk
11	20.288	0.555	RR	CELL	1	FF_X35_Y11_N9	std_2s60ES:inst|z_pwm_0:the_z_pwm_0|pwm_avalon_interface:z_pwm_0|pwm_task_logic:task_logic|lpm_divide:Div0|lpm_divide_jkm:auto_generated|sign_div_unsign_bnh:divider|alt_u_div_aaf:divider|StageOut[318]~181_OTERM535_Duplicate_Duplicate
12	20.670	0.382					clock pessimism

	Total	Incr	RF	Type	Fanout	Location	Element
3	20.650	-0.020					clock uncertainty
4	20.668	0.018		uTsu	1	FF_X35_Y11_N9	std_2s60ES:inst|z_pwm_0:the_z_pwm_0|pwm_avalon_interface:z_pwm_0|pwm_task_logic:task_logic|lpm_divide:Div0|lpm_divide_jkm:auto_generated|sign_div_unsign_bnh:divider|alt_u_div_aaf:divider|StageOut[318]~181_OTERM535_Duplicate_Duplicate